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EXAMINER	
SORRELL, ERON J	
ART UNIT	PAPER NUMBER
2182	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/618,041	BURTON, LEE A.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59 and 61-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-30,32-59,61-72 and 76-85* is/are rejected.

7)☐ Claim(s) *7,31 and 73-75* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/29/06 has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is

shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-41 and 48-62 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-37 of copending Application No. 09/932,330. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the instant application recite limitations using the term "dense logic device," while the claims of application 09/932,330 use the term "processor" to describe the same functional unit. The independent claims of the instant application also recite the limitation of "a direct execution logic element" coupled to an adapter port that is associated with a memory module slot while the claims of 09/932,330 recite "a processor element associated" with a memory module slot to describe the same structure. Finally the independent claims of the instant application recite the limitation of memory resources being included in the adaptor port. While not explicitly set forth in the claims of 09/932,330, one of ordinary skill in the art would realize the processor element

associated with the adaptor port claimed would use registers to hold data for manipulation.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6,9,12,18-20,26-30,33,36,48-50,56,61-63,67-69,71,72,84, and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent No. 6,052,134) in view of Klingelhofer (U.S. Patent No. 5,673,204).

6. Referring to claims 1 and 26, Foster teaches a computer system (see figure 1) comprising:

at least one dense logic device (see item 12 of figure 1);

an interleaved controller (see item 14 in figure 2 and lines 1-8 of column 2 and lines 11-37 of column 7) for coupling the at least one dense logic device to a control block (see item 28 in figure 1) and a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one memory module slot (see lines 30-55 of column 5).

Foster fails to teach the system further an adaptor port associated with the at least one memory module slot the adapter port including associated memory resources substantially equally accessible by the dense logic device and the at least one direct execution logic element coupled to the adapter port.

Klingelhofer teaches a computer system comprising the above limitations (see item 120 in figure 1), and suggests the adaptor port (IOSIMM), is located in an available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of Klingelhofer. One of ordinary skill in the art would have been motivated to make such modification in order to quickly operate on I/O data as if they were in system memory as suggested by Klingelhofer (see lines 29-40 of column 5).

The combination of Foster and Klingelhofer fails to teach an adapter port associated with at least two of the plurality of memory slots.

It would have been obvious to one of ordinary skill in the art to modify at the time of the applicant's invention to modify the combination of Foster and Klingelhofer such that the it comprises an adapter port associated with at least two of the memory slots in order to connect and interface with more external devices.

7. Referring to claim 56, Foster teaches a computer system including, the computer system comprising at least one dense logic device coupled to said memory bus (see item 12 in figure 1 and bus coupled memory 18).

Foster fails to teach an adapter port for electrical coupling between a memory bus of said computer system and a network interface said adapter port comprising: a memory resource associated with said adapter port; and a control block for selectively enabling access by said at least one dense logic device to said memory resource.

Klingelhofer teaches a computer system comprising the above limitations (see item 120 in figure 1), and suggests the adaptor

port (IOSIMM), is located in an available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of Klingelhofer. One of ordinary skill in the art would have been motivated to make such modification in order to quickly operate on I/O data as if they were in system memory as suggested by Klingelhofer (see lines 29-40 of column 5).

8. Referring to claim 2, Foster teaches the controller is an interleaved memory controller (see item 14 in figure 2 and lines 1-8 of column 2 and lines 11-37 of column 7) that is bi-directionally coupled to the at adaptor port and said one or more memory module slots (see item MD-72 in figure 3), and wherein said controller includes a plurality of control registers configured to control shared use of said memory resources (see item 88 in figure 3).

9. Referring to claims 3,27,68, Foster teaches the plurality of memory module slots comprise DIMM memory module slots (see lines of column; Note DIMMs have a 64-bit width and Foster discloses the memory banks disclosed have a 64-bit width).

10. Referring to claims 4,5,6,28,29,30,61,62, and 69, Foster teaches DIMM slots (which are in=line memory modules) as shown above and Klingelhofer teaches the adapter port comprises an in-line memory physical format for retention within one of the in-line memory module slots.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of Klingelhofer. One of ordinary skill in the art would have been motivated to make such modification for the same reasons as mentioned above.

11. Referring to claims 9 and 33, Foster teaches the control block comprises a peripheral bus control block (see item labeled 20 in figure 1).

12. Referring to claims 12 and 36, Foster teaches the control block comprises a graphics control block (see item labeled 20 in figure 1).

13. Referring to claims 18 and 48 Klingelhofer teaches the direct execution logic element comprises a reconfigurable processor element (see lines 20-27 of column 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Foster with the above teachings of Klingelhofer in order to modify the operation of the adapter port.

14. Referring to claims 19,20,49, and 50, Klingelhofer teaches the processor element is operative to alter data received from the external device prior to transmission on the memory module bus (see lines 20-26 of column 5) and the direct execution logic element is operative to alter data received from the external device prior to transmission on the memory module bus (see lines 20-26 of column 5, note the bi-directional communication links).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of Klingelhofer in order for the data to be in the proper format/protocol for sending and receiving data.

15. Referring to claim 63, Klingelhofer teaches the claimed adapter port.

It would have been obvious to one of ordinary skill in the art the time of the applicant's invention to add an additional

adapter port that performs the same function to allow for greater external device connections.

16. Referring to claim 67, Foster teaches the memory bus comprises first and second memory module slots (see lines 30-55 of column 5) and Klingelhofer teaches the adaptor port is configured to physical retention in the memory module slot (see lines 7-41 of column 7).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the teachings of Klingelhofer for the same reasons as outlined in the rejection of claim 56, supra.

17. Referring to claim 71, Foster teaches the computer system comprises a memory and I/O controller interposed between said at least one dense logic device and said memory bus (see item 14 in figure 1).

18. Referring to claim 72, Foster the memory and I/O controller comprises an interleaved memory controller (see lines 1-8 of column 2).

19. Referring to claims 76 and 77, Foster as modified by Klingelhofer teaches the memory bus provides address/control and data inputs to said control block to at least partially control its functionality (see lines 7-18 of column 7).

20. Referring to claims 84 and 85, Klingelhofer teaches the memory resource comprises VRAMs, which are simply DRAMs that store video data (see item 70 in figure 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the teachings of O'Sullivan for the same reasons as outlined in the rejection of claim 56, supra.

21. Claims 8,10,11,13,14,32,34,35,37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of Klingelhofer as applied to claims 1 and 26 above, and further in view of Mays, Jr. (U.S. Patent No. 6,452,700).

22. Referring to claims 8,10,11,13,14,32,34,35,37, and 38 the combination of Foster and Klingelhofer fails to teach the graphics control block provides control information to the direct execution logic element of the adapter port (note the graphics control block is also a peripheral bus control block).

Mays, Jr. teaches an I/O control block which provides control information to the direct execution logic element of the adapter port (see lines 20-42 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the above teachings of Mays, Jr. One of ordinary skill in the art would have been motivated to make such modification in order to facilitate in data transfers as suggested by Mays, Jr. (see lines 20-42 of column 4).

23. Claims 15-17 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of Klingelhofer as applied to claims 1 and 26 above, and further in view of Whittaker et al. (U.S. Patent No. 5,889,959 hereinafter "Whittaker").

24. Referring to claims 15-17 and 39-41 the combination of Foster and Klingelhofer fails to teach the control block comprises systems maintenance control block, wherein the systems maintenance control block provides control information to the direct execution logic element of the adapter port.

Whittaker teaches a control block comprising a systems maintenance control block, wherein the systems maintenance control block provides control information said adapter port (see lines 42-49 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the above teachings of Whittaker. One of ordinary skill in the art would have been motivated to make such modification in order to provide diagnostic functions to all of the modules in the system as suggested by Whittaker (see lines 30-43 of column 1).

25. Claims 22-24, and 52-54 rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of Klingelhofer as applied to claims 1 and 26 above, and further in view of Chiles et al. (U.S. Patent No. 6,581,157 hereinafter "Chiles").

26. Referring to claims 21,51, and 70, the combination of Foster and Klingelhofer fails to teach the direct execution element comprises a control block coupled to the adapter port.

Chiles teaches an adapter port comprising a direct execution element comprises a control block coupled to the adapter port (see item 252 in figure 3). The control block on

the adapter port allows for the device to be upgraded with removing or replacing the device (see paragraph bridging columns 7 and 8). For this reason, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the above teachings of Chiles.

27. Referring to claim 22,23,52, and 53 the combination of Foster and Klingelhofer fails to teach the direct execution logic element further comprises at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said adapter port and a read only memory associated with said control block for providing configuration information thereto, and wherein the system further comprising a dual-ported memory block coupling a control block coupled to said adapter port to said at least one field programmable gate array.

Chiles teaches the above limitation (see item labeled 256 in figure 3 and paragraph bridging columns 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the teachings of Chiles. One of ordinary skill would have been motivated to make

such modification in order to upgrade the adapter port without purchasing a new one.

28. Referring to claims 24 and 54 the combination of Foster and Klingelhofer fails to teach the processor element comprises a chain port for coupling the processor element to another processor element.

Chiles teaches the processor element comprises a chain port for coupling the processor element to another processor element (see paragraph bridging columns 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the teachings of Chiles. One of ordinary skill in the art would have been motivated to make such modification in order to connect the host computer to a network.

29. Referring to claim 25 and 55 Chiles teaches the direct execution element comprises a read only memory associated with the control block for providing configuration information thereto (see item 254 in figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the

combination of Foster and Klingelhofer with the above teachings of Chiles for the same reasons as mentioned in the rejection of claims 22,23,52, and 53.

30. Referring to claims 57 and 64, Chiles teaches the control block is further operational to selectively preclude access by said at least one dense logic device to said memory resource (see lines 9-31 of column 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the teachings of Chiles for the same reasons as mentioned above.

31. Referring to claim 58,65, and 83, Klingelhofer teaches the at least one direct execution logic element coupled to said network interface (see item DX in figure 1 coupled to a device separate from the computer).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the teachings of O'Sullivan for the same reasons as outlined in the rejection of claim 56, supra.

32. Referring to claims 59 and 66, Chiles teaches the control block is further operational to selectively preclude access by said at least one dense logic device to said memory resource (see lines 9-31 of column 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the teachings of Chiles for the same reasons as mentioned above.

33. Claims 42-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of Klingelhofer as applied to claim 1 above, and further in view PCI Technology Overview (hereinafter "PCITO").

34. Referring to claims 42-47 the combination of Foster and Klingelhofer fails to teach the control block comprises a PCI-X or PCI-Express control block, wherein the PCI-X or PCI-Express control block provides control information to the direct execution logic element of the adapter port.

PCITO teaches a control block comprising a PCI-X or PCI-Express control block wherein the PCI-X or PCI-Express control block provides control information said adapter port (see pages 12,13, and 16).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the above teachings of PCITO. One of ordinary skill in the art would have been motivated to make such modification in order to useful in high speed networking environments or high-speed chip interconnects as suggested by PCITO (see pages 8 and 16).

35. Claims 78-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of Klingelhofer as applied to claim 1 above, and further in view FreeBSD Developers' Handbook Chapter 9.

36. Referring to claims 78-82, the combination of Foster and Klingelhofer fails to teach the control block further comprises a DMA controller providing fully parameterized direct memory access operations memory resource, wherein the DMA controller enables scatter/gather, irregular data access pattern functions, and data packing functions to be implemented.

FreeBSD Developers' Handbook Chapter 9, teaches such a DMA controller that can perform the above functions (see section 9.1).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and Klingelhofer with the above teachings form FreeBSD Developers' Handbook Chapter 9, in order to relieve the direct execution logic element of the burden of transferring data as suggested by FreeBSD Developers' Handbook Chapter 9 (see section 9.1).

Allowable Subject Matter

37. Claims 7,31, and 73-75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

38. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach or suggest, alone or in combination, with respect to claims 7 and 31, the adaptor port monitoring the control block for control information when the controller is disconnected from the memory resources, in combination with the other recited claim elements; and with respect to claims 73-75, a number of switches interposed between said memory bus and said memory resource controllable by said control block, the switches

comprise field effect transistors, the computer switches have condition thereof coupling said dense device to said memory resource and second condition thereof for coupling said network interface said memory resource, in combination with the other recited claim elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
November 28, 2007

11/28/07